CLAIMS

1. A semiconductor device comprising:

an integrated circuit including a first thin film transistor and a second thin film transistor; and

an antenna electrically connected to the integrated circuit,

wherein one of a source region and a drain region of the second thin film transistor connects to a gate electrode of the second thin film transistor,

wherein the first thin film transistor is formed from a first region of a semiconductor film,

wherein the second thin film transistor is formed from a second region of the semiconductor film, and

wherein the first region is superior to the second region in crystallinity.

2. A semiconductor device comprising:

an integrated circuit including a first thin film transistor and a second thin film transistor; and

an antenna electrically connected to the integrated circuit, wherein the integrated circuit comprises:

a memory cell;

15

25

a microprocessor; and

at least one of a connection terminal, a rectifier circuit for producing a power supply voltage from an alternating signal input into the connection terminal by the antenna, a demodulator circuit for forming a signal by demodulating the alternating signal, and a modulator circuit for modulating a load applied to the antenna by controlling a switch based on data read from the memory cell by the signal,

wherein the first thin film transistor is formed in the microprocessor,

wherein the first thin film transistor is formed from a first region of a semiconductor film,

30 wherein the second thin film transistor is formed in the memory cell,

5

10

15

20

25

30

wherein the second thin film transistor is formed from a second region of the semiconductor film,

wherein one of a source region and a drain region of the second thin film transistor connects to a gate electrode of the second thin film transistor, and

wherein the first region is superior to the second region in crystallinity.

3. A semiconductor device comprising:

an integrated circuit including a first thin film transistor and a second thin film transistor; and

an antenna electrically connected to the integrated circuit,

wherein one of a source region and a drain region of the second thin film transistor connects to a gate electrode of the second thin film transistor,

wherein the first thin film transistor is formed from a first region of a semiconductor film,

wherein the second thin film transistor is formed from a second region of the semiconductor film,

wherein the first region comprises a crystal grain grown continuously in one direction, and

wherein the second region comprises a crystal grain having a diameter in a range from a half of a channel length of the second thin film transistor to three times of the channel length thereof.

4. A semiconductor device comprising:

an integrated circuit including a first thin film transistor and a second thin film transistor; and

an antenna connected to the integrated circuit,

wherein the integrated circuit comprises:

a memory cell;

a microprocessor; and

one of a connection terminal, a rectifier circuit for producing a power supply

5

15

20

voltage from an alternating signal input into the connection terminal by the antenna, a demodulator circuit for forming a signal by demodulating the alternating signal, and a modulator circuit for modulating a load applied to the antenna by controlling a switch based on data read from the memory cell by the signal,

wherein the first thin film transistor is formed in the microprocessor,

wherein the first thin film transistor is formed from a first region of a semiconductor film,

wherein the second thin film transistor is formed in the memory cell,

wherein the second thin film transistor is formed from a second region of the semiconductor film,

wherein one of a source region and a drain region of the second thin film transistor connects to a gate electrode of the second thin film transistor,

wherein the first region comprises a crystal grain grown continuously in one direction, and

wherein the second region comprises a crystal grain having a diameter in a range from a half of a channel length of the second thin film transistor to three times of the channel length thereof.

5. A semiconductor device according to any one of claims 3 and 4,

wherein an active layer of the first thin film transistor is arranged so that the one direction conforms to a direction in which an electric carrier moves.

6. A semiconductor device comprising:

an integrated circuit including a first thin film transistor and a second thin film transistor, and

an antenna electrically connected to the integrated circuit,

wherein one of a source region and a drain region of the second thin film transistor connects to a gate electrode of the second thin film transistor,

wherein the first thin film transistor is formed from a first region of a semiconductor film crystallized by a continuous wave laser,

WO 2005/081303 PCT/JP2005/003225

48

wherein the second thin film transistor is formed from a second region of the semiconductor film, and

wherein the first region is superior to the second region in crystallinity.

7. A semiconductor device comprising:

an integrated circuit including a first thin film transistor and a second thin film transistor; and

an antenna connected to the integrated circuit, wherein the integrated circuit comprises:

10 a memory cell;

5

15

20

25

a microprocessor; and

at least one of a connection terminal, a rectifier circuit for producing a power supply voltage from an alternating signal input into the connection terminal by the antenna, a demodulator circuit for forming a signal by demodulating the alternating signal, and a modulator circuit for modulating a load applied to the antenna by controlling a switch based on data read from the memory cell by the signal,

wherein the first thin film transistor is formed in the microprocessor,

wherein the first thin film transistor is formed from a first region of a semiconductor film crystallized by a continuous wave laser,

wherein the second thin film transistor is formed in the memory cell,

wherein the second thin film transistor is formed from a second region of the semiconductor film,

wherein one of a source region and a drain region of the second thin film transistor connects to a gate electrode of the second thin film transistor, and

wherein the first region is superior to the second region in crystallinity.

8. A semiconductor device according to any one of claims 6 and 7,
wherein the first region includes a crystal grain grown continuously in a
scanning direction of the continuous wave laser.

9. A semiconductor device according to claim 8,

wherein an active layer of the first thin film transistor is arranged so that the scanning direction conforms to a direction in which an electric carrier moves.

10. A semiconductor device according to any one of claims 6 to 9,

wherein the second region includes a crystal grain having a diameter in a range from a half of a channel length of the second thin film transistor to three times of the channel length thereof. -

11. A method for manufacturing a semiconductor device, comprising:

forming a semiconductor film having an amorphous structure over a first substrate;

irradiating the semiconductor film with a laser beam with scanning in a direction, thereby forming a first region and a second region in the semiconductor film; and

forming an integrated circuit comprising a first thin film transistor using the first region in the semiconductor film and a memory cell array comprising a second thin film transistor using the second region in the semiconductor film,

wherein the first region is superior to the second region in crystallinity.

20

15

5

10

- 12. A method for manufacturing a semiconductor device according to claim 11, wherein the integrated circuit comprises:
 - a memory cell;
 - a microprocessor; and
- at least one of a connection terminal, a rectifier circuit, a demodulator circuit and a modulator circuit,
- 13. A method for manufacturing a semiconductor device according to claim 11, wherein the second thin film transistor comprises a gate electrode, a source region and a drain region, and

WO 2005/081303 PCT/JP2005/003225

wherein the gate electrode is electrically connected to one of the source region and the drain region.

- 14. A method for manufacturing a semiconductor device according to claim 11,5 further comprising forming an antenna.
 - 15. A method for manufacturing a semiconductor device according to claim 14, wherein the step of forming the integrated circuit and the memory cell array comprises a process of forming a gate electrode, and

wherein the step of forming the antenna is performed at the same time as the process of forming the gate electrode.

16. A method for manufacturing a semiconductor device according to claim 14, wherein the step of forming the integrated circuit and the memory cell array comprises a process of forming one of a source electrode and a drain electrode, and wherein the step of forming the antenna is performed at the same time as the process of forming the one of the source electrode and the drain electrode.

17. A method for manufacturing a semiconductor device according to claim 11,20 further comprising:

forming an antenna over a second substrate; and

attaching the first substrate to the second substrate so as to sandwich the integrated circuit, the memory cell array and the antenna between the first substrate and the second substrate.

25

10

15

18. A method for manufacturing a semiconductor device according to claim 11, wherein the laser beam is a continuous wave laser beam, and wherein the first region includes a crystal grain grown continuously in the direction of scanning the continuous wave laser beam.

19. A method for manufacturing a semiconductor device according to claim 11, wherein an active layer of the first thin film transistor is arranged so that the direction of scanning the laser beam conforms to a direction in which an electric carrier moves in the active layer when electric current is flown in the first transistor.

5

- 20. A method for manufacturing a semiconductor device according to claim 11, further comprising:
- forming a base-film over the first substrate before forming the semiconductor film;
- forming a stripping layer over the base film before forming the semiconductor film;
 - stripping the integrated circuit and the memory cell array from the first substrate; and
- attaching the stripped integrated circuit and the memory cell array to a second substrate.
 - 21. A method for manufacturing a semiconductor device according to claim 11, wherein the first substrate is selected from the group consisting of glass substrate, a quartz substrate, a ceramic substrate and a metal substrate.

20

22. A method for manufacturing a semiconductor device according to claim 20, wherein the second substrate is flexible and selected from the group consisting of a paper substrate and a plastic substrate.

25

- 23. A method for manufacturing a semiconductor device according to claim 20, wherein the step of stripping the integrated circuit and the memory cell array from the first substrate comprises:
- forming a groove in a peripheral region of the integrated circuit and the memory cell array so as to expose the base film through the stripping layer;
- flowing an etching gas into the groove, thereby removing the stripping layer.